

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Attorney Docket No.: 249/246

In re patent application of:

Group Art Unit: 2814

Sug-hun HONG

Serial No. (Unassigned)

Div of 09/324,929

Examiner: A. Mai

Filed: April 26, 2001

For: TRENCH ISOLATION METHOD

**PRELIMINARY AMENDMENT**

Commissioner for Patents  
United States Patent and Trademark Office  
Washington, D.C. 20231

Sir:

Prior to examination on the merits, please amend the above-identified  
application as follows:

103470-00000000

IN THE CLAIMS:

Please cancel claims 1-8, 10-24 and 26-29.

Kindly replace claim 9 with the following claim 9 written in independent format:

9. (Amended) A trench isolation method comprising:

forming a trench in a semiconductor substrate using a mask pattern defining an active area;

sequentially stacking an oxide layer and a nitride pad layer on the sidewall of the trench and forming an insulation layer in the trench;

removing the mask pattern down to the upper surface of the semiconductor substrate of the active area; and

forming a capping layer of an insulating material, the capping layer filling a recess at the upper edge of the trench, the recess generated by etching the nitride pad layer formed on the sidewalls of the trench during removing the mask pattern,

wherein the capping layer is formed by forming an insulating material by self epitaxial growth (SEG), and then removing the insulating material layer down to the upper surface of the semiconductor substrate of the active area so that only the insulating material layer filled in the recess is exposed.

The changes in the previous claim are indicated by brackets for deletions and underlining for insertions.

9. (Amended) A trench isolation method comprising:

forming a trench in a semiconductor substrate using a mask pattern defining an active area;

sequentially stacking an oxide layer and a nitride pad layer on the sidewall of the trench and forming an insulation layer in the trench;

removing the mask pattern down to the upper surface of the semiconductor substrate of the active area; and

forming a capping layer of an insulating material, the capping layer filling a recess at the upper edge of the trench, the recess generated by etching the nitride pad layer formed on the sidewalls of the trench during removing the mask pattern.[.]

[The trench isolation method of claim 1,]

wherein the capping layer is formed by forming an insulating material by self epitaxial growth (SEG), and then removing the insulating material layer down to the upper surface of the semiconductor substrate of the active area so that only the insulating material layer filled in the recess is exposed.

Kindly replace claim 25 with the following claim 25 written in independent format.

25. (Amended) A trench isolation method comprising:

forming a trench in a semiconductor substrate using a mask pattern defining an active area;

sequentially stacking a first oxide layer, a nitride pad layer and a second oxide layer on the sidewall of the trench and forming an isolation layer in the trench;

removing the mask pattern to expose the upper surface of the semiconductor substrate of the active area; and

forming a capping layer of an insulating material, the capping layer filling a recess at the upper edge of the trench recess generated by etching the nitride pad layer formed on the sidewalls of the trench during removal of the mask pattern,

wherein the capping layer is formed by forming an insulating material layer by self epitaxial growth (SEG), and then removing the insulating material layer down to the upper surface of the semiconductor substrate of the active area so that only the insulating material layer filled in the recess is exposed.

The changes in the previous claim are indicated by brackets for deletions and underlining for insertions.

25. (Amended) A trench isolation method comprising:

forming a trench in a semiconductor substrate using a mask pattern defining an active area;

sequentially stacking a first oxide layer, a nitride pad layer and a second oxide layer on the sidewall of the trench and forming an isolation layer in the trench;

removing the mask pattern to expose the upper surface of the semiconductor substrate of the active area; and

forming a capping layer of an insulating material, the capping layer filling a recess at the upper edge of the trench recess generated by etching the nitride pad layer formed on the sidewalls of the trench during removal of the mask pattern,[]

[The trench isolation method of claim 15,]

wherein the capping layer is formed by forming an insulating material layer by self epitaxial growth (SEG), and then removing the insulating material layer down to the upper surface of the semiconductor substrate of the active area so that only the insulating material layer filled in the recess is exposed.

IN THE SPECIFICATION:

Kindly insert the following new paragraph and heading prior to the section entitled, "Background of the Invention," on page 2:

**RELATED APPLICATION**

This application is a divisional of United States Patent Application Serial No. 09/324,929, filed June 3, 1999, now United States Patent No. \_\_\_\_\_.

Serial No.:

Attorney Docket No. 249,246

Divisional of 09/324,919

---

IN THE DRAWINGS:

Please enter new drawings 3A and 3B.

REMARKS

The undersigned attorney awaits favorable action on the merits.

Respectfully submitted,



Eugene M. Lee, Reg. No. 32,039

Richard A. Sterba, Reg. No. 43,162

Date April 26, 2001

THE LAW OFFICES OF EUGENE M. LEE, PLLC  
2111 WILSON BOULEVARD, SUITE 1200  
ARLINGTON, VA 22201  
703.525.0978 TEL  
703.525.4265 FAX

FIG. 3A

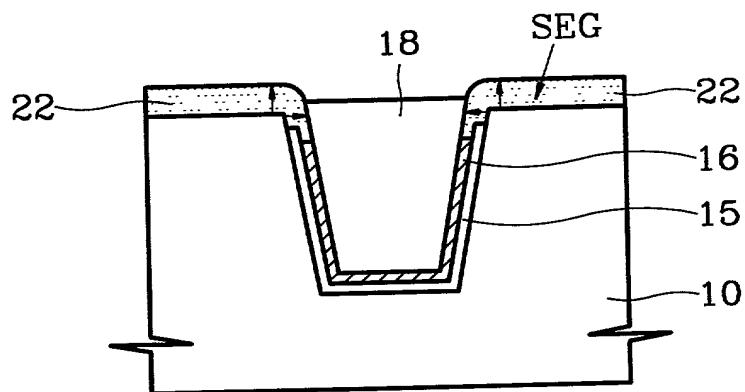


FIG. 3B

